CLAIMS

1. A method of incorporating a dielectric material into a semiconductor device, said semiconductor device being fabricated by a process that includes at least one thermal processing step at a temperature greater than a maximum withstand temperature of said dielectric material, said method comprising:

fabricating said semiconductor device at least up to the thermal processing step using a further dielectric material having a maximum withstand temperature greater than the temperature of the thermal processing step;

removing at least a portion of said further dielectric material; and

depositing a layer of said lower withstand temperature dielectric material in place of the removed portion of said further dielectric material.

2. The method of claim 1 wherein said lower withstand temperature dielectric material has a lower dielectric constant than said further dielectric material.

3. The method of claim 1 wherein said further dielectric material includes a portion that is disposed adjacent to at least one conductive line of said semiconductor device.

4. The method of claim 3 wherein said at least one conductive line includes a contact barrier layer, and the thermal processing step is an anneal step of said contact barrier layer.

5. The method of claim 3 wherein an etch stop layer is disposed beneath said further dielectric material; and wherein said step of removing at least a portion of said further dielectric material includes etching down to said etch stop layer.

6. The method of claim 3 wherein said step of removing at least a portion of said further dielectric material includes a timed etching step.

7. The method of claim 3 further comprising:

planarizing said said lower withstand temperature dielectric material to a top surface of said conductive line;

depositing a further layer of said lower withstand temperature dielectric material atop said layer of said said lower withstand temperature dielectric material and atop said conductive line.

8. The method of claim 3 wherein said step of depositing a layer of said lower withstand temperature dielectric material includes depositing said layer atop said conductive line; and said method further includes planarizing said layer of said lower withstand temperature dielectric material such that a portion thereof remains atop said conductive line and serves as an inter-level dielectric layer.

9. A method of incorporating a dielectric material into an insulator structure that is adjacent to at least one conductive line of a semiconductor device, said insulator structure and said conductive line being fabricated by a process that includes at least one thermal processing step at a temperature greater than a maximum withstand temperature of said dielectric material, said method comprising:

fabricating said insulator structure and said conductive line at least up to the thermal processing step using a further dielectric material that has a maximum withstand temperature greater than the temperature of the thermal processing step;

removing at least a portion of said further dielectric material; and

depositing a layer of said lower withstand temperature dielectric material in place of the removed portion of said further dielectric material.

10. The method of claim 9 wherein said fabricating step includes:

depositing a layer of a first dielectric material atop a surface of a semiconductor substrate;

planarizing said first dielectric material to a top surface of another conductive line disposed atop said semiconductor substrate;

depositing a layer of a further dielectric material atop said first dielectric layer and atop said another conductive line;

patterning and etching said further dielectric material and said first dielectric material to form at least one opening therein; and

filling said opening with at least one conducting material to form said at least one conductive line.

11. The method of claim 9 wherein said lower withstand temperature dielectric material has a lower dielectric constant than said further dielectric material.

12. The method of claim 9 wherein said step of fabricating said insulator structure and said conductive line includes: depositing a contact barrier layer prior to depositing said conductive line, and annealing said contact barrier layer at a temperature greater than said maximum withstand temperature of said lower withstand temperature dielectric material.

13. The method of claim 9 wherein an etch stop layer is disposed beneath said further dielectric material; and wherein said step of removing at least a portion of said further dielectric material includes etching down to said etch stop layer.

14. The method of claim 9 wherein said step of removing at least a portion of said further dielectric material includes a timed etching step.

15. The method of claim 9 further comprising:

planarizing said layer of said lower withstand temperature dielectric material to a top surface of said conductive line;

depositing a further layer of said lower withstand temperature dielectric material atop said layer of said another dielectric material and atop said conductive line.

16. The method of claim 9 wherein said step of depositing a layer of said lower withstand temperature dielectric material includes depositing said layer atop said conductive line; and said method includes planarizing layer of said lower withstand temperature dielectric material such that a portion thereof remains atop said conductive line and serves as an inter-level dielectric layer.

17. A method of fabricating a semiconductor device, said method comprising:

forming at least one deep trench within a semiconductor substrate;

forming a buried plate within a region of said semiconductor substrate that adjoins a bottom of said deep trench;

forming an insulator film along sidewalls of said deep trench;

removing an upper region of said insulator film;

partly filling said deep trench with doped polysilicon that extends above a remaining portion of said insulator film, the dopants in the polysilicon diffusing through at least one side of said deep trench into an adjoining region of said semiconductor substrate during subsequent thermal processing steps to form a buried strap region along said side of said deep trench;

forming a trench top oxide layer atop said doped polysilicon;

forming a gate insulator layer on at least said upper portion of said side of said deep trench;

filling said deep trench with a further polysilicon layer atop said trench top oxide layer;

patterning and etching said semiconductor substrate to form at least one isolation trench that adjoins said deep trench;

filling said isolation trench with an insulator material;

forming a doped region in a top surface of said semiconductor substrate adjacent to said gate insulator layer of said deep trench;

forming a contact region that connects to said further polysilicon layer;

depositing at least one conducting layer atop said contact region to form a first conductive line;

depositing a layer of a first dielectric material atop said surface of said semiconductor substrate;

planarizing said first dielectric layer to said top surface of said first conductive line;

depositing a layer of a further dielectric material atop said first dielectric layer and atop said first conductive line;

patterning and etching said further dielectric layer and said first dielectric layer to form at least one opening therein that includes at least one region that extends down to said doped region adjacent to said gate dielectric;

depositing a contact barrier layer at least at a bottom of said opening;

annealing said contact barrier layer;

filling said opening with at least one further conducting layer to form at least one further conductive line;

removing at least an upper portion of said further dielectric layer to form at least one opening adjacent to said further conductive line; and

depositing a layer of another dielectric material at least in said opening adjacent to said bit line, said another dielectric material having a lower dielectric constant than that of said further dielectric material.

18. The method of claim 17 wherein said annealing step is carried out at a temperature greater than a maximum withstand temperature of said another dielectric material.

19. The method of claim 17 further comprising: depositing an etch stop layer atop said first dielectric layer prior to depositing said layer of a further dielectric

material; and wherein said step of removing at least an upper portion of said further dielectric material includes etching down to said etch stop layer.

20. The method of claim 17 wherein said step of removing at least an upper portion of said further dielectric material includes a timed etching step.

21. The method of claim 17 further comprising:

planarizing said another dielectric layer to a top surface of said bit line;

depositing a further layer of said another dielectric material atop said layer of said another dielectric material and atop said further conductive line.

22. The method of claim 17 wherein said step of depositing a layer of another dielectric material includes depositing said layer of another dielectric material atop said further conductive line; and said method further comprises planarizing said another dielectric layer such that a portion thereof remains atop said further conductive line and serves as an inter-level dielectric layer.

23. A method of fabricating a semiconductor device, said method comprising:

forming a planar gate oxide layer atop a surface of a semiconductor substrate;

depositing at least one conducting layer atop said gate oxide layer;

patterning and etching said at least one conducting layer to form at least two openings therein;

introducing dopants into said substrate through said openings in said at least one conducting layer to form at least one source region and at least one drain region;

depositing a layer of a first dielectric material atop said surface of said semiconductor substrate;

planarizing said first dielectric material to said top surface of said at least one conducting layer line;

depositing a layer of a further dielectric material atop said first dielectric layer and atop said at least one conductive layer;

patterning and etching said further dielectric layer and said first dielectric layer to form at least one opening therein that includes at least one region that extends down to at least one of said source region and said drain region;

depositing a contact barrier layer at least at a bottom of said opening;

annealing said contact barrier layer;

filling said opening with at least one further conducting layer;

removing at least an upper portion of said further dielectric layer to form at least one opening adjacent to said further conducting layer; and

depositing a layer of another dielectric material at least in said opening adjacent to said further conductive layer, said another dielectric material having a lower dielectric constant than that of said further dielectric material.

24. The method of claim 23 wherein said annealing step is carried out at a temperature greater than a maximum withstand temperature of said another dielectric material.

25. The method of claim 23 further comprising: depositing an etch stop layer atop said first dielectric layer prior to depositing said layer of a further dielectric material; and wherein said step of removing at least an upper portion of said further dielectric material includes etching down to said etch stop layer.

26. The method of claim 23 wherein said step of removing at least an upper portion of said further dielectric material includes a timed etching step.

27. The method of claim 23 further comprising:

planarizing said another dielectric layer to a top surface of said further conductive layer;

depositing a further layer of said another dielectric material atop said layer of said another dielectric material and atop said further conducting layer.

28. The method of claim 23 wherein said step of depositing a layer of another dielectric material includes depositing said layer of another dielectric material atop said further conducting layer; and said method further comprises planarizing said another dielectric layer such that a portion thereof remains atop said further conducting layer and serves as an inter-level dielectric layer.

29. A semiconductor device incorporating a dielectric material into an insulator structure that is adjacent to at least one conductive line, said insulator structure and said conductive line being fabricated by a process that includes at least one thermal processing step at a temperature greater than a maximum withstand temperature of said dielectric material, said process comprising:

fabricating said insulator structure and said conductive line at least up to the thermal processing step using a further dielectric material that has a maximum withstand temperature greater than the temperature of the thermal processing step;

removing at least a portion of said further dielectric material; and

depositing a layer of said lower withstand temperature dielectric material in place of the removed portion of said further dielectric material.

30. The semiconductor device of claim 29 wherein said fabricating step includes:

depositing a layer of a first dielectric material atop a surface of a semiconductor substrate;

planarizing said first dielectric material to a top surface of an insulated word line disposed atop said semiconductor substrate;

depositing a layer of a further dielectric material atop said first dielectric layer and atop said insulated word line;

patterning and etching said further dielectric material and said first dielectric material to form at least one opening therein; and

filling said opening with at least one conducting material to form at least one bit line.

31. The semiconductor device of claim 29 wherein said lower withstand temperature dielectric material has a lower dielectric constant than said further dielectric material.

32. The semiconductor device of claim 29 wherein said step of fabricating said insulator structure and said bit line includes: depositing a contact barrier layer prior to depositing said conductive line, and annealing said contact barrier layer at a temperature greater than said maximum withstand temperature of said lower withstand temperature dielectric material.

33. The semiconductor device of claim 29 wherein an etch stop layer is disposed beneath said further dielectric material; and wherein said step of removing at least a portion of said further dielectric material includes etching down to said etch stop layer.

34. The semiconductor device of claim 29 wherein said step of removing at least a portion of said further dielectric material includes a timed etching step.

35. The semiconductor device of claim 29 further comprising:

planarizing said layer of said lower withstand temperature dielectric material to a top surface of said bit line;

depositing a further layer of said lower withstand temperature dielectric material atop said layer of said another dielectric material and atop said conductive line.

36. The semiconductor device of claim 29 wherein said step of depositing a layer of said lower withstand temperature dielectric material includes depositing said layer atop said conductive line; and said process includes planarizing layer of said lower withstand temperature dielectric material such that a portion thereof remains atop said conductive line and serves as an inter-level dielectric layer.

37. A semiconductor device fabricated by a process comprising:

forming at least one deep trench within a semiconductor substrate;

forming a buried plate within a region of said semiconductor substrate that adjoins a bottom of said deep trench;

forming an insulator film along sidewalls of said deep trench;

removing an upper region of said insulator film;

partly filling said deep trench with doped polysilicon that extends above a remaining portion of said insulator film, the dopants in the polysilicon diffusing through at least one side of said deep trench into an adjoining region of said semiconductor substrate during subsequent thermal processing steps to form a buried strap region along said side of said deep trench;

forming a trench top oxide layer atop said doped polysilicon;

forming a gate insulator layer on at least said upper portion of said side of said deep trench;

filling said deep trench with a further polysilicon layer atop said trench top oxide layer;

patterning and etching said semiconductor substrate to form at least one isolation trench that adjoins said deep trench;

filling said isolation trench with an insulator material;

forming a doped region in a top surface of said semiconductor substrate adjacent to said gate insulator layer of said deep trench;

forming a contact region that connects to said further polysilicon layer;

depositing at least one conducting layer atop said contact region to form a first conductive line;

depositing a layer of a first dielectric material atop said surface of said semiconductor substrate;

planarizing said first dielectric layer to said top surface of said first conductive line;

depositing a layer of a further dielectric material atop said first dielectric layer and atop said insulated word line;

patterning and etching said further dielectric layer and said first dielectric layer to form at least one opening therein that includes at least one region that extends down to said doped region adjacent to said gate dielectric;

depositing a contact barrier layer at least at a bottom of said opening;

annealing said contact barrier layer;

filling said opening with at least one further conducting layer to form at least one further conductive line;

removing at least an upper portion of said further dielectric layer to form at least one opening adjacent to said bit line; and

depositing a layer of another dielectric material at least in said opening adjacent to said bit line, said another dielectric material having a lower dielectric constant than that of said further dielectric material.

38. The semiconductor device of claim 37 wherein said annealing step is carried out at a temperature greater than a maximum withstand temperature of said another dielectric material.

39. The semiconductor device of claim 37 further comprising: depositing an etch stop layer atop said first

dielectric layer prior to depositing said layer of a further dielectric material; and wherein said step of removing at least an upper portion of said further dielectric material includes etching down to said etch stop layer.

40. The semiconductor device of claim 37 wherein said step of removing at least an upper portion of said further dielectric material includes a timed etching step.

41. The semiconductor device of claim 37 further comprising:

planarizing said another dielectric layer to a top surface of said further conductive line;

depositing a further layer of said another dielectric material atop said layer of said another dielectric material and atop said further conductive line.

42. The semiconductor device of claim 37 said step of depositing a layer of another dielectric material includes depositing said layer of another dielectric material atop said further conductive line; and said process further comprises planarizing said another dielectric layer such that a portion thereof remains atop said further conductive line and serves as an inter-level dielectric layer.

43. A semiconductor device fabricated by a process comprising:

forming a planar gate oxide layer atop a surface of a semiconductor substrate;

depositing at least one conducting layer atop said gate oxide layer;

patterning and etching said at least one conducting layer to form at least two openings therein;

introducing dopants into said substrate through said openings in said at least one conducting layer to form at least one source region and at least one drain region;

depositing a layer of a first dielectric material atop said surface of said semiconductor substrate;

planarizing said first dielectric layer to said top surface of said conducting layer;

depositing a layer of a further dielectric material atop said first dielectric layer and atop said conducting layer;

patterning and etching said further dielectric layer and said first dielectric layer to form at least one opening therein that includes at least one region that extends down to said source and drain regions;

depositing a contact barrier layer at least at a bottom of said opening;

annealing said contact barrier layer;

filling said opening with at least one further conducting layer;

removing at least an upper portion of said further dielectric layer to form at least one opening adjacent to said further conducting layer; and

depositing a layer of another dielectric material at least in said opening adjacent to said further conductive layer, said another dielectric material having a lower dielectric constant than that of said further dielectric material.

44. The semiconductor device of claim 43 wherein said annealing step is carried out at a temperature greater than a maximum withstand temperature of said another dielectric material.

45. The semiconductor device of claim 43 further comprising: depositing an etch stop layer atop said first dielectric layer prior to depositing said layer of a further dielectric material; and wherein said step of removing at least an upper portion of said further dielectric material includes etching down to said etch stop layer.

46. The semiconductor device of claim 43 wherein said step of removing at least an upper portion of said further dielectric material includes a timed etching step.

47. The semiconductor device of claim 43 further comprising:

planarizing said another dielectric layer to a top surface of said further conductive layer;

depositing a further layer of said another dielectric material atop said layer of said another dielectric material and atop said further conducting layer.

48. The semiconductor device of claim 43 wherein said step of depositing a layer of another dielectric material includes depositing said layer of another dielectric material atop said further conducting layer; and said process further comprises planarizing said another dielectric layer such that a portion thereof remains atop said further conducting layer and serves as an inter-level dielectric layer.

49. A semiconductor device comprising:

at least one deep trench formed within a semiconductor substrate;

a buried plate formed within a region of said semiconductor substrate and adjoining a bottom of said deep trench;

an insulator film formed along a lower portion of sidewalls of said deep trench;

doped polysilicon partly filling said deep trench and extending above said insulator film;

a buried strap region disposed along at least one side of said deep trench and adjoining said doped polysilicon;

a trench top oxide layer disposed atop said doped polysilicon;

a gate insulator layer formed on at least said upper portion of said side of said deep trench;

a further polysilicon layer disposed atop said trench top oxide layer and filling said deep trench with;

at least one isolation trench formed in said semiconductor substrate and adjoining said deep trench;

said isolation trench being filled with an insulator material;

a doped region formed in a top surface of said semiconductor substrate adjacent to said gate insulator layer of said deep trench;

a first conductive line disposed atop and connecting to said further polysilicon layer, said first conductive line being formed of at least one conducting layer;

a first dielectric layer extending from said surface of said semiconductor substrate to said top surface of said first conductive line;

a further dielectric layer disposed atop said first dielectric layer and atop said first conductive line and having at least one opening therein that includes at least one region that extends down to said doped region adjacent to said gate dielectric;

an annealed contact barrier layer formed at least at a bottom of said opening; and

at least one conducting material filling a reminder of said opening to form at least one further conductive line;

at least an upper portion of said further dielectric layer being a material having a lower dielectric constant than that of a remaining portion of said further dielectric layer and having maximum withstand temperature lower than a temperature at which said contact barrier layer is annealed.

50. The semiconductor device of claim 49 wherein said upper portion of said further dielectric layer is disposed atop said further conductive line and serves as an inter-level dielectric layer.

51. A semiconductor device comprising:

a planar gate oxide layer disposed atop a surface of a semiconductor substrate;

at least one conducting layer formed atop said gate oxide layer and having at least two openings therein;

at least one source region and at least one drain region disposed in said substrate beneath said openings in said at least one conducting layer;

a first dielectric layer extending from said surface of said semiconductor substrate to said top surface of said at least one conducting layer;

a further dielectric layer disposed atop said first dielectric layer and atop said at least one conducting layer and having at least one opening therein that includes at least one region that extends down to at least one of said source region and said drain region;

an annealed contact barrier layer formed at least at a bottom of said opening; and

at least one further conducting layer filling a reminder of said opening;

at least an upper portion of said further dielectric layer being a material having a lower dielectric constant than that of a remaining portion of said further dielectric layer and having maximum withstand temperature lower than a temperature at which said contact barrier layer is annealed.

52. The semiconductor device of claim 51 wherein said upper portion of said further dielectric layer is disposed atop said further conducting layer and serves as an inter-level dielectric layer.